OFFICE OF NAVAL RESEARCH

PUBLICATIONS/PATENTS/PRESENTATIONS/HONORS REPORT

for

1 October 1992 through 30 September 1993

for

Contract N00014-91-J-1852

VLSI for High-Speed Digital Signal Processing

Principal Investigator: Professor Alan N. Willson, Jr.

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OFFICE OF NAVAL RESEARCH
PUBLICATION/PATENTS/PRESENTATION/HONORS REPORT
for
1 Oct 92 through 30 Sept 93

R&T Number: 414-8503-03

Contract/Grant Number: N00014-91-J-1852

Contract/Grant Title: VLSI for High-Speed Digital Signal Processing

Principal Investigator: Alan N. Willson, Jr.

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Phone Number (with Area Code): (310)825-7400

E-Mail Address: willson@ee.ucla.edu

a. Number of Papers Submitted to Referred Journal but not yet published: 2

b. Number of Papers Published in Referred Journals: 1
(list attached)

c. Number of Books or Chapters Submitted but not yet Published: 0

d. Number of Books or Chapters Published: 1
(list attached)

e. Number of Printed Technical Report & Non-Referred Papers: 0
(list attached)

f. Number of Patents Filed: 1

g. Number of Patents Granted: 0
(list attached)

h. Number of Invited Presentations at Workshops or Prof. Society Meetings: 0

i. Number of Presentation at Workshop or Prof. Society Meetings: 5

j. Honors/Awards/Prizes for Contract/Grant Employees:
(list attached, this might Include Scientific Soc. Awards/Offices, Promotions, Faculty Award/Offices etc.)

k. Total number of Graduate Students and Post-Docs Supported at least 25%, this year on this contract,grant:
Grad Students 5 and Post Docs 0

How many of each are females or minorities? (These 6 numbers are for ONR's EEO/Minority Reports; minorities Include Blacks, Aleuts Amindians, etc and those of Hispanic or Asian extraction/nationality. This Asians are singled out to facilitate meeting the varying report semantics re "under-represented")

- Grad Student Female 1
- Grad Student Minority 0
- Grad Student Asian e/n 2
- Post-Doc Female 0
- Post-Doc Minority 0
- Post-Doc Asian e/n 0

(a.) **Papers Submitted to Refereed Journals (and not yet published)**

M. J. Werter and A. N. Willson, Jr., "Automated Programming of Digital Filters for Parallel Processing Implementation," submitted to *IEEE Trans. on Circuits and Systems*, 1992. (ONR, MICRO)

A. Y. Kwentus, H-T. Hung, and A. N. Willson, Jr., "An Architecture for High-Performance/Small-Area Multipliers for Use in Digital Filtering Applications," submitted to *IEEE J. of Solid State Circuits,* 1993. (ONR, MICRO)

(b.) **Published Papers in Refereed Journals**

B-R. Horng, H. Samueli, and A. N. Willson, Jr., "The Design of Two-Channel Lattice-Structure Perfect-Reconstruction Filter Banks Using Powers-of-Two Coefficients," to appear in July 1993 issue of *IEEE Transactions on Circuits and Systems - I.*

(c.) **Books or Chapters Submitted for Publication**

None.

(d.) **Books or Chapters Published**

Chapter: A Ring-Structured Topology of Programmable Digital Filter Processors on a Single Chip, pp. 195-240, in *VLSI Signal Processing, V.* IEEE, edited by K. Yao and R. Jain, 1992.

(e.) **Printed Technical Reports and Non-Refereed Papers**

None.

(f.) **Patents Filed**

A Programmable Digital Signal Processor Using Switchable Unit-Delays for Optimal Hardware Allocation (Patent filed, April 1993)

(g.) **Patents Granted**

None.

(h.) **Invited Presentations at Workshops or Professional Society Meetings**

None.

(i) **Contributed Presentations at Workshops or Professional Society Meetings**

A. Y. Kwentus, M. J. Werter and A. N. Willson, Jr., "A Ring-Structured Topology of Programmable Digital Filter Processors on a Single Chip," *Proc. of the 1992 IEEE International Workshop on VLSI Signal Processing*, Napa Valley, CA, October 28-30, 1992, pp. 195-204. (ONR, MICRO).

K-Y. Khoo, A. Kwentus, and A. N. Willson, Jr., "An Efficient 175 MHz Programmable FIR Digital Filter," *Proc. of 1993 IEEE International Symposium on Circuits and Systems*, Chicago, IL, May 3-6, 1993, pp. 72-75. (ONR, NSF)

A. Y. Kwentus, H-T. Hung, and A. N. Willson, Jr., "High-Performance/Small-Area Multipliers for use in Digital Filtering Applications," *Proc. of the 36th Midwest Symposium on Circuits and Systems*, Detroit, MI, August 16-18, 1993. (ONR, MICRO)

A. Y. Kwentus, M. J. Werter, and A. N. Willson, Jr., "A Programmable Digital Filter IC Employing Multiple Processors on a Single Chip," *Proc. of the International Conference on Signal Processing Applications & Technology '93*, Santa Clara, CA, September 27-October 1, 1993. (ONR, MICRO)

K-Y. Khoo, A. Kwentus, and A. N. Willson, Jr., "An Efficient 175 MHz Programmable FIR Digital Filter," *Proc. of the International Conference on Signal Processing Applications & Technology '93*, Santa Clara, CA, September 27-October 1, 1993. (ONR, NSF)

(j.) **Honors/Awards/Prizes**

Appointed Chair of IEEE Circuits and Systems Society's CAS Transactions Prize Paper Awards Committee.

Quarterly Progress Report

(July 1, 1993 through September 30, 1993)

on

VLSI for High-Speed Digital Signal Processing

prepared for

Office of Naval Research
800 North Quincy Street
Arlington, VA 22217-5000

Scientific Officer: Dr. Clifford Lau

Grant No.: N00014-91-J-1852
R & T Project: 4148503-03

Principal Investigator:

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VLSI for High-Speed Digital Signal Processing

Quarterly Progress Report – 7/1/93 through 9/30/93

During the past quarter we have completed the testing of our recently fabricated single-processor IC. This is the last "preliminary chip" we intend to fabricate before fabricating our full five-processor ring IC. Its primary purpose is to verify that all aspects of our ALU, program and coefficient RAMs, and Register Blocks are functioning correctly. The chip provides for 11-bit input and output data with 16-bit internal data and 11-bit coefficients (stored in on-chip memory). The chip also has an 8-bit microprocessor bus interface for loading programs and coefficients. The IC contains 25,000 transistors and occupies an area of 14.8 mm^2 (3.7 mm by 4.0 mm including pads) in 1.2-μm CMOS technology. A block diagram of the chip is shown in Figure 1.

Of the 24 parts that we fabricated through MOSIS, 19 were found to be fully functional and all 19 functional parts operated at an instruction clock rate greater than 50 MHz with a 5V supply voltage. The Tektronix LV500 Chip Tester that we have been using to test our chip can only operate up to a 50 MHz clock rate. Thus, at the present time we are unable to determine the maximum operating frequency at a 5V supply voltage. Figure 2 shows the test results for the minimum supply voltage at which the chip will operate at 50 MHz. Figure 3 shows the test results for operation with a 3.3 V supply voltage. Due to LV500 tester limitations we can only test the chip's operating frequency in 4 ns steps.

We have also tested the chip by programming it to implement several filters. (While this is a preliminary test-chip, it can also be viewed as a fully functional one-processor "ring.")

Figure 4 shows the transfer function of a 15-tap lowpass FIR filter which was implemented and run on the chip at a 50 MHz instruction clock rate. The filter requires 15 program steps, so the data rate is 3.33 MHz (only 3 steps will be required on the five-processor ring, yielding a data rate of 16.67 MHz). We have also programmed a cascade of two second-order IIR filter sections. This IIR filter requires 10 program steps on the single-processor IC, so the data rate is 5 MHz (only 2 program steps will be required on the five-processor ring IC, yielding a data rate of 25 MHz).

We have made considerable progress on the design and layout of the five-processor ring IC. This IC will have five of our processors arranged in a ring with a dual-port register block between each processor. Figure 5 shows the top level block diagram of this IC. Each of the processors is identical to the processor fabricated on the single-processor IC and each of the register blocks is identical to one of the two register blocks included on the single-processor IC. This five-processor IC will be pin-for-pin compatible with the single-processor IC we have already fabricated. Thus, it will be a "drop in" replacement for the single-processor IC on the demonstration board we are developing. We expect to fabricate the five-processor ring IC in 0.8-μm CMOS through MOSIS during the 1st quarter of 1994.

Two IBM PC boards which have been designed to demonstrate the capabilities of the ring processor have now been successfully built and tested. The two boards, which interface directly to the IBM PC bus, allow for the computer hosting the boards to upload image files for two-dimensional filtering, or a data file for one-dimensional filtering. The first board (see Figure 6) contains four of our ring-processor ICs, a PC bus interface, and several

state-machines for control of the data paths. The second board (see Figure 7) contains a large RAM bank for storing images and the necessary blocking and control circuitry for implementing two-dimensional processing using our ring processor chips on the first board. The boards also allow an external data source to be fed to the processors for higher speed processing. Both boards have been debugged and tested. A custom software package is now being written which will allow the user to upload images and data files, as well as to program the processors in a user friendly manner.

We have presented a paper entitled "High-Performance/Small-Area Multipliers for Use in Digital Filtering Applications" at the 1993 Midwest Symposium on Circuits and Systems in Detroit August 16-18, 1993. A copy of the paper is included with this report. We have also presented two papers at the International Conference on Signal Processing Applications & Technology in Santa Clara, CA, Sept. 28 - Oct. 1, 1993. One paper, entitled "A Programmable Digital Filter IC Employing Multiple Processors on a Single Chip," describes our ring processor IC. The other paper, entitled "An Efficient 175 MHz Programmable FIR Digital Filter," describes the programmable FIR chip that we reported on in a previous progress report, and on which UCLA has filed for a patent.

The paper entitled "Automated Programming of Digital Filters for Parallel Processing Implementation," which describes the ONR-supported development of a computer algorithm for automatically writing optimal programs for the implementation of arbitrary digital filter structures on our ring-of-processors IC, was accepted for publication by the *IEEE Trans. on Circuits and Systems.* This paper's publication has been delayed some-

what due to the unusual backlog situation that this journal is presently experiencing. In addition, our ONR-supported paper entitled "The Design of Two-Channel Lattice-Structure Perfect-Reconstruction Filter Banks Using Powers-of-Two Coefficients," will appear in the July 1993 issue of the *IEEE Trans. on Circuits and Systems*, however only galley proofs (copy enclosed) are presently available.

The UCLA M.S. thesis of Michael C. Kennedy was approved, and the M.S. degree was awarded. This thesis project involved the design of a VLSI silicon compiler to generate a 16×16-bit parallel multiplier with extendible word lengths for digital filter applications. It included the ONR-supported MOSIS fabrication of a state-of-the-art multiplier IC. The work will be of value for our group's future research projects.

Another ONR-supported MS thesis project, that of Linda Ying, has required two MOSIS fabrication runs. We expect Linda to finish her work this fall. She is implementing an efficient "prefilter" IC for use with the above-mentioned programmable FIR filter chip, to form a prefilter-equalizer cascade structure of the type reported by Adams and Willson.

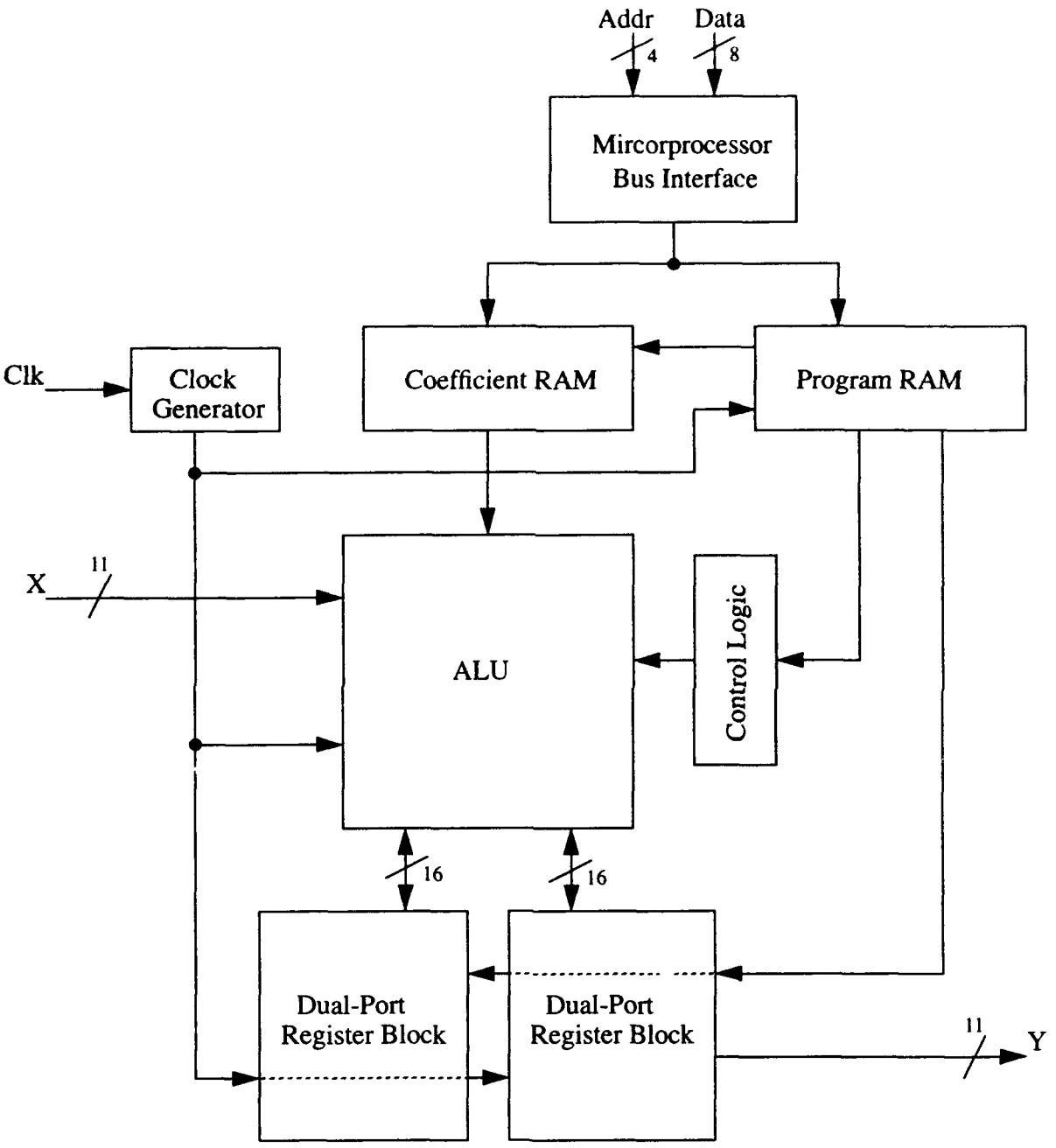

Figure 1 - Single-Processor IC Block Diagram

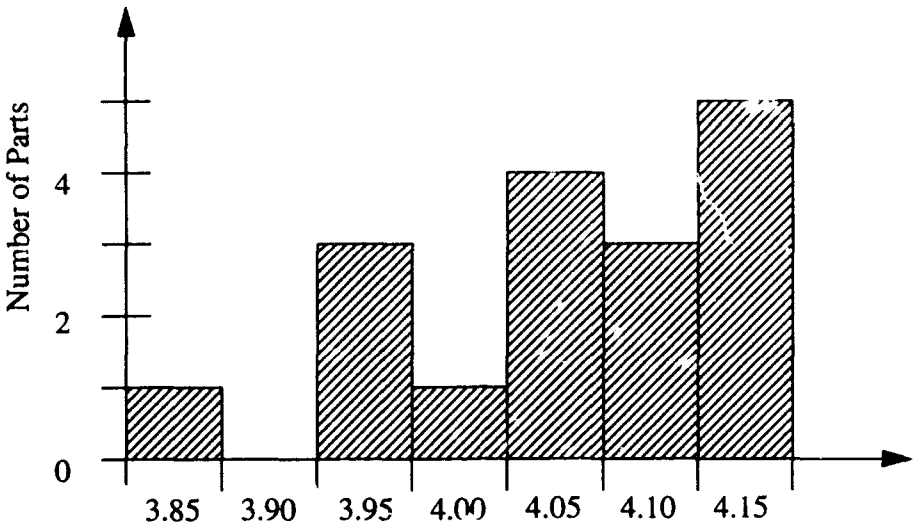

Figure 2 - Minimum Supply Voltage for 50 MHz Operation (V)

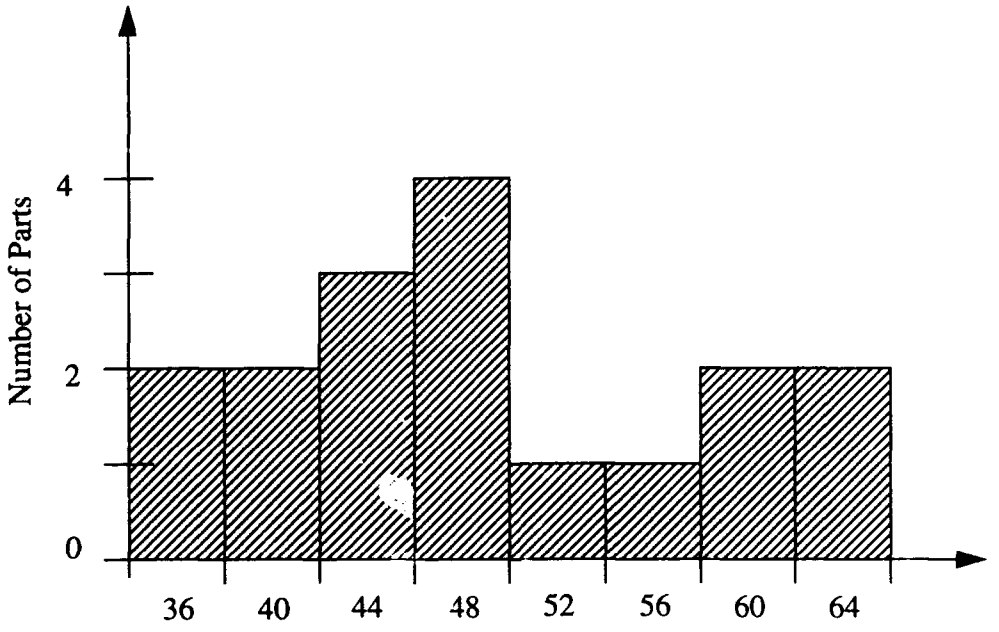

Figure 3 -Minimum Clock Cycle for 3.3V-Supply (ns)

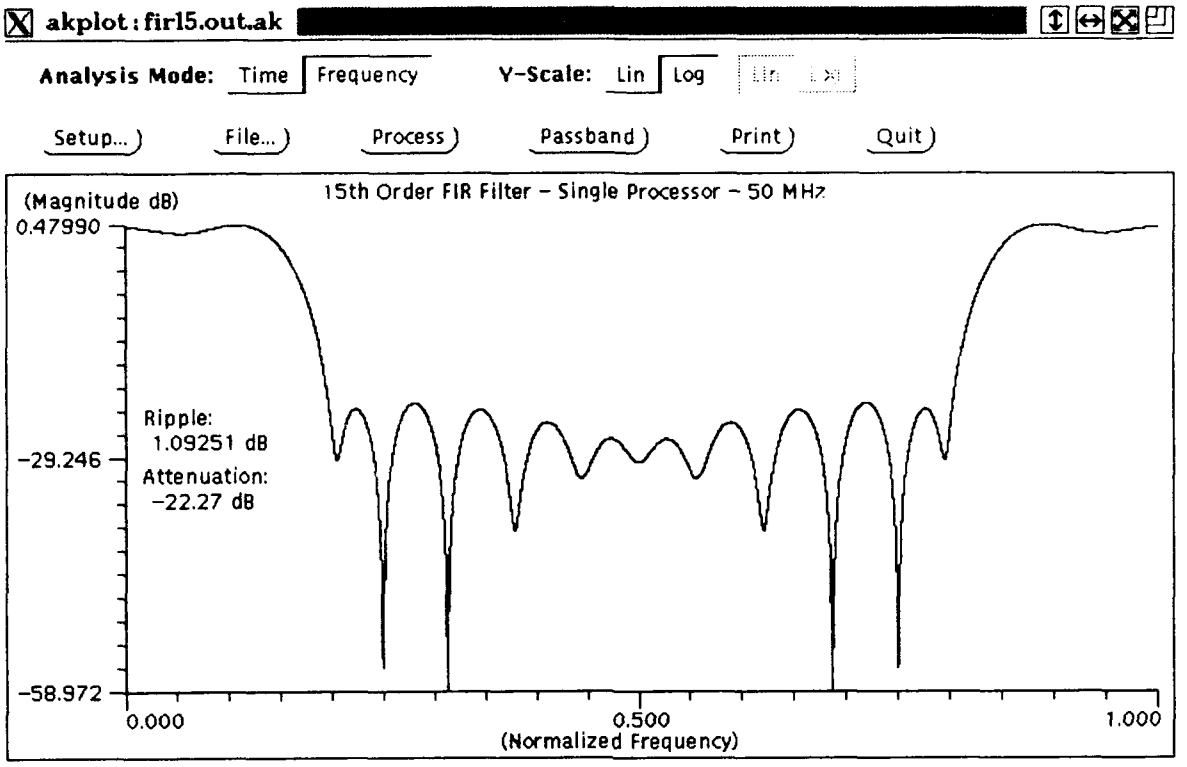

Figure 4 -Transfer Function of 15-tap FIR Filter

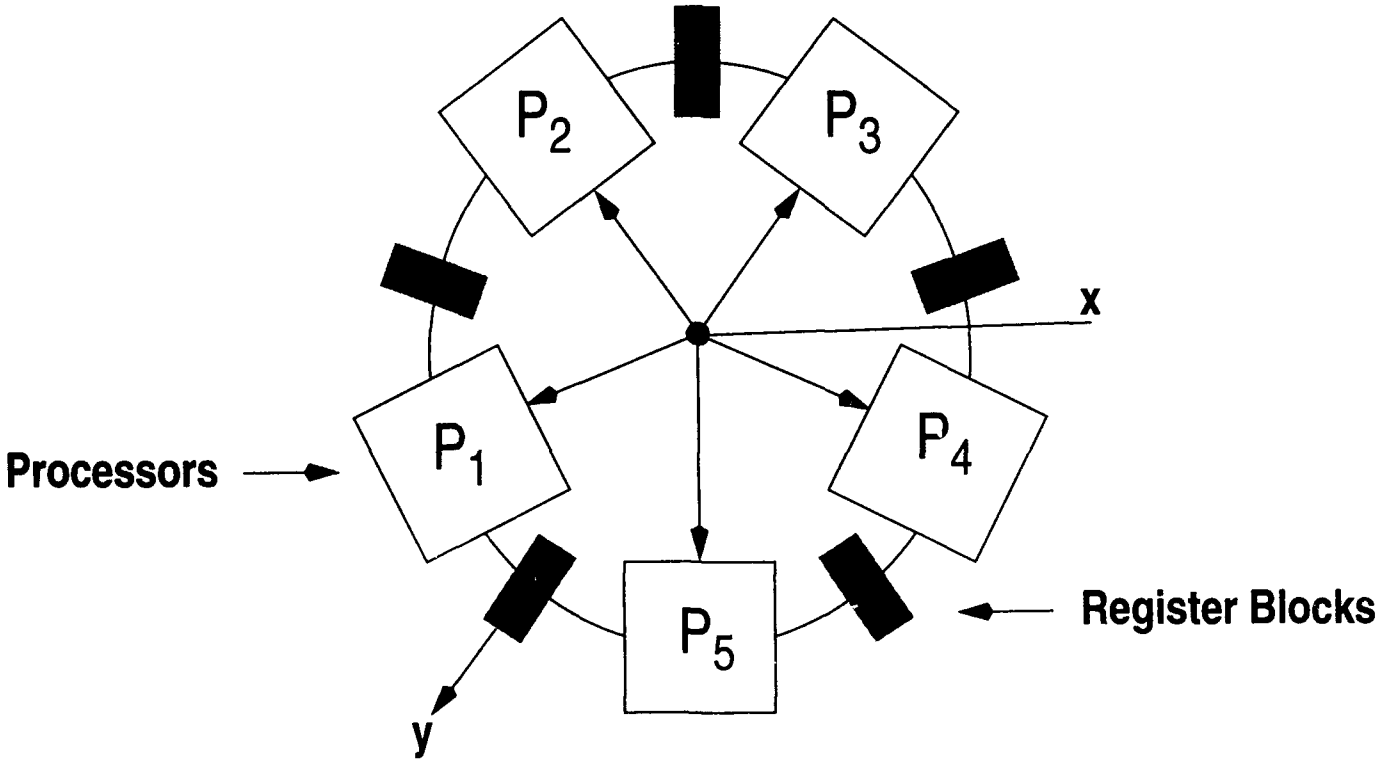

Figure 5 - Five-Processor Ring IC Block Diagram

Four of our single-processor ICs (each as illustrated in Fig. 1). To later be replaced with four of our 5-processor ring ICs. (Each as illustrated in Fig. 5).

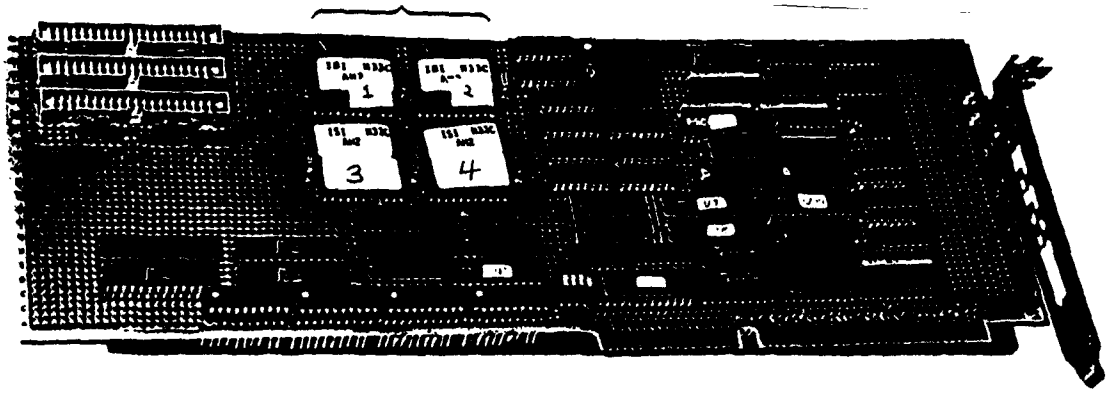

Figure 6 – Processor Board.

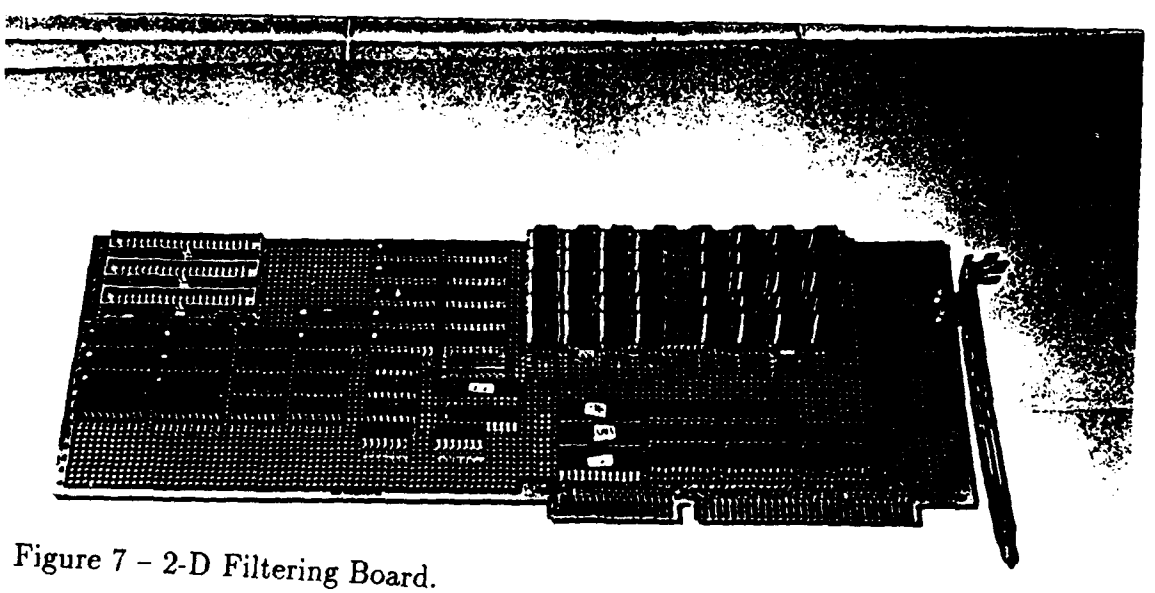

Figure 7 – 2-D Filtering Board.